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MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
CAMPOS, YAIMA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

CONTINUATION OF 11

Amendment presented to claim 27 requires further consideration and/or search.

Rejections Under 35 USC 112, First Paragraph (Claims 1-9 and 24)

Since the amendment filed on 8/3/2010 has not been entered, the 112 rejections of claims 1-9 and 24 have been maintained for the reasons pointed out in the final rejection mailed on 6/7/20/10.

Rejections Under 35 USC 103(a) – Goldberg and Lehman (Claims 10, 12-15 and 26-27)

Applicant argues that "there is no motivation to combine Lehman with Goldberg because Goldberg explicitly criticizes and discredits... multiple buffer pool implementations... linked lists " as taught by Lehman.

In response, these arguments have been fully considered, but they are not deemed persuasive since while Goldberg points out certain disadvantages of buffer pools and linked lists, Lehman's invention is not directed to these specific buffer pools or linked lists but is directed to a bitmap 120 to indicate memory availability (See fig. 7 and related text). Further, Goldberg's preferred embodiments are also directed to the use of bitmaps to indicate memory availability (Refer to Abstract).

The Examiner would also like to point out that the reference to Goldberg does not teach away from the possibility of combining Goldberg with Lehman to obtain the claimed invention as Goldberg's disclosure does not criticize, discredit, or otherwise discourage the solution claimed *In re Fulton,* 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004). See also MPEP 2123. For example, Goldberg, in the Background

section describes different methods for tracking and allocating available memory in a computer system wherein Goldberg explains that **["The use of multiple buffer pools allows storage resources to be allocated in a manner that conserves system resources. However, depending on the number of pools created within the system, more memory may still be allocated than is necessary... which results in a considerable waste of storage space" (col. 2, lines 26-35)]**; thus, contrary to Applicant's assertion, Goldberg is not criticizing, discrediting or discouraging the use of multiple buffer pools for the allocation of available memory, but is merely explaining a specific situation in which more memory than is necessary is allocated using buffer pools, which results in waste of storage. Further, note that Goldberg is not criticizing, discrediting or discouraging the particular invention of Lehman or any modification resulting from combining Goldberg with Lehman, but is merely discussing particular solutions to a given problem that are alternate to the preferred embodiments of Goldberg.

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Goldberg and Lehman are involved and directed to memory access and control, more specifically, optimizing memory allocation by indicating available/unavailable memory wherein one of ordinary skill in the art would recognize that modifying Goldberg as taught by Lehman would provide the advantages of **["a data space management system that requires less space**

to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions" (Col. 2, lines 42-48)].

Applicant argues the combination does not disclose "… the first state of the first logic circuit comprises a number of available memory segments… nowhere in Goldber is there any teaching that bit 612 indicates that 6 memory sections in Bitmap 2 606 are available. As such, the first state of bit 612 does not comprise a number of available memory segments in the first memory block…".

In response, these arguments have been fully considered but they are not deemed persuasive since there is no limitation or requirement in the claims dictating that the "the first state of the first logic circuit comprises a number of available memory segments" include for example, "6" as argued by Applicant. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The combination of Goldberg and Lehman discloses "wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to the first state of the second logic circuit" and "wherein the first sate of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit" as Goldberg discloses **[bitmap 1 (*corresponding the claimed first logic circuit*) wherein each state in bitmap 1 corresponds to a number of sections of memory pointed to by LLB (*which comprises a second logic circuit comprising a first state and a separate***

***and third logic circuit comprising a first state*) (See fig. 6 and related text of Goldberg), wherein Goldberg further discloses "a bitmap structure is defined that allows N contiguous search items to be located wherein all search items in the set have a same predetermined attribute. The system and method may be adapted for use in locating N contiguous sections of memory all having the same predetermined attribute. Namely the contiguous sections are all available for allocation" (Col. 8, line 23-32) wherein figure 6 teaches each state of a higher level bitmap comprises an available number of memory portions in a lower level bitmap (fig. 6 and related text; col. 4, lines 4-56). Applicant should note, that every bit of Bitmap 1 comprises a number of available memory sections/segments in LLB; wherein the Bitmap hierarchy depicted comprises more levels such as Bitmap 2 and Bitmap 3 (Fig. 6 and related text)]**; however, Goldberg is not explicit in reciting the first sate of bitmap 1 comprising a number of available memory segments.

Lehman explicitly discloses wherein a state of a logic circuit comprises a number of available memory segments in the first memory block, <u>said number of available memory segments corresponding to the first state of the second logic circuit</u> or to the state of a logic circuit indicating availability of memory segments as [**"for the first type of bit map, where the size bit is set to size=1, the bits are examined as individual bits, and logical groups inside the 16 bits must be determined by examining adjacent bits. For example, for size=1, the pattern 1100 1111 0011 0000 shows a free block of size 2 at address 2, a free block of size 2 at address 8, and a free block of size 4 at address 12. The size of a set of free blocks is implicit in the number of free unit blocks-they are never subdivided" (Col. 11, lines 6-14) and further discloses "as the**

buddy segments... are allocated... the count array 122 and the pointer array 124 are updated to indicate the current count of free blocks" (col. 10, lines 11-25; fig. 7 and related text)]. Thus, clearly discloses bits indicating availability of memory comprise a number of available/free portions of memory. Therefore, in view of Lehman's disclosure, one of ordinary skill in the art would appreciate that each bit of bitmap 1 of Goldberg comprises a number of sections of memory pointed to by the LLB which comprises 1 bit to indicate availability or unavailability of memory sections.

Applicant argues the combination does not teach "…wherein the second state of the first logic circuit comprises an offset to available memory... Lehman merely... provide a place to start looking for a segment of a particular size…".

In response, these arguments have been fully considered, but they are not deemed persuasive. The combination of Goldberg and Lehman discloses "wherein the second state of the first logic circuit comprises an offset to available memory" as Lehman discloses **["pointer array 124 permit the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and provide a place to start looking for a segment of a particular size" (Col. 9, lines 53-60) wherein "the pointer array 124 might point to a buddy segment that is available). Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least a correct starting point for a search for that size buddy segment" (Col. 10, lines 1-10) (Figure 7 and related text)]**; *wherein Applicant should note that in case that the offset points to an available memory segment, the offset comprises "an offset to available*

memory" and in case that the memory segment has been allocated and the offset has not been allocated, then the offset comprises an offset to a location to start looking for available memory; thus, Lehman discloses the claimed limitation of an offset to available memory and more, since in the case that for some reason this memory is no longer available the offset still points to a place where to start looking for available memory, which comprises "an offset to available memory". Further, the pending claims do not contain any requirement or limitation precluding the offset as taught by the combination of Goldberg and Lehman from reading on the claimed "offset to available memory."

Additionally, claim 27 requires information indicating an offset to available memory and the response presented on the non-final office action mailed on 11/5/2009 regarding claim 27 still applies to the rejection of claim 27.

/Yaima Campos/
Examiner, Art Unit 2185

/Tuan V. Thai/
Primary Examiner, Art Unit 2185